Qualification Report

AH103

The Communications Edge ™

Product Information

I. SUMMARY

The WJ AH103 passed all Qualification requirements as described in this report. The parameters monitored for each of the qualification tests were Supply Current (Idss), Gain, 3rd Order Output Intercept Point (OIP3) and 1dB Compression Point (P1dB). Failures are defined as any variation of 2 dB or greater for P1dB or a variation of 10% or greater for the other measured parameters as compared to the initial pre-stressed testing. The results of the individual qualification tests are located in Section V. There were no major anomalies during any of the tests except for HAST where an inductor failed on the bias line to one of the devices. This is described in further detail in Section VI.8.

II. SCOPE

The AH103 is a ½ Watt, high gain, high linearity amplifier containing two discrete GaAs die packaged in a "down-set" (DS) SOIC-8 package. Both GaAs die, the HDO3 and HD07, have been successfully qualified in SOT89 packages as the WJ AM1 and the WJ AH102 single chip devices, respectively. The goal of this qualification effort is to prove the reliability of the two GaAs die when molded in the DS SOIC-8 package using a higher performance molding compound and performing at a higher total device power dissipation since two die are operating together in the same package.

III. APPLICABLE DOCUMENTS

Test procedures and methods are consistent with industry standard Joint Electron Device Engineering Council (JEDEC) requirements. Each individual JEDEC Specification is referenced next to each Qualification Test in the table provided in Section IV below.

IV. QUALIFICATION TEST PLAN AND RESULTS

Stress or Test	Procedures / Conditions	Device Hours/ Cycles	Sample Size	Failed Units	Date	Reference Document	Part Tested
Preconditioning Level 1	External visual 40x High temp storage life: 24 hrs @ +125°C Temp. & Humidity Test 168 hrs. @ +85°C / 85% RH Infrared Solder Reflow (IR) test 3 cycles w/flux immersion, peak temp: 235°C	N/A	3 lots, a total of 960 parts (used for TC, UA, & HAST tests)	N/A	Q1 2003	JESD22-A113 JESD22-A101 JESD22-B101 JESD22-103 JESD22-A112.4	AH103
Temperature Cycle	Test Condition C Temp. -65° C to +150° C Dwell time = 10 to 15 min.	1000 cycles	3 lots, 77 parts per lot	0	Q2 2003	JESD22-A104-B	AH103
Unbiased Autoclave	Test Condition C Temp. 121°C, 15 psig, RH = 100%	96 hours	3 lots, 77 parts per lot	0	Q1 2003	JESD22-A102-C	AH103
Unbiased High Temperature Storage	Temp. 150° C	1000 hours	1 lot, 77 total parts	0	Q2 2003	JESD22-A108-B	AH103
Highly-Accelerated Temperature & Humidity Stress Test (HAST)	Test Condition A Temp. 130°C, 33.3 psig, RH = 85%	96 hours	3 lots, 77 parts per lot	1*	Q1 2003	JESD22-A110-A	AH103
High Temp Op Life (HTOL)	Test Condition B Temp. 125°C (+5, -0°C)	1,000 hours	3 lots, 77 parts per lot	0	Q2 2003	JESD22-A108-B	AH103
Electrostatic Discharge (ESD)	Charged Device Model (CDM)	N/A	15 total parts	Class III	Q2 2003	JESD22-C101-A	AH103
	Human Body Model (HBM)	N/A	15 total parts	Class 1B		JESD22-A114	AH103
Physical Dimensions	N/A	N/A	1 lot, 10 parts per lot	N/A	Q2 2003	JESD22-B100-A	AH103

* Please refer to Section VI.8 for further information.

V. STRESS AND TEST METHODOLOGY

Qualifications tests for HTOL and HAST were performed with the AH103 surface mount re-flowed to a Qualification PCB. All other Qualification tests were performed on loose parts. The PCB layout contains 15 individual circuits nearly identical to the 900 MHz Application Circuit published in the WJ Communications' AH103 Data Sheet, using the recommended via pattern. One qualification PCB is reserved, as a control board. This control board is never exposed to any environment and is tested before and after each set of the stressed devices to ensure measurement accuracy and repeatability. Acceptance criterion consists of having zero or one failure out of 77 parts to meet WJCI's requirement of LTPD = 5 (Lot Tolerance Percent Defective) for each test. Failures are defined as any variation of 2 dB or greater for P1dB or a variation of 10% or greater for the other measured parameters as compared to the initial pre-stressed testing.

VI. DISCUSSION OF RESULTS

1. **Pre-Conditioning**
   A total of 960 AH103 devices (3 lots) completed pre conditioning.

2. **Temperature Cycle**
   A total of 230 AH103 devices (3 lots) passed Temperature Cycle with no failures or anomalies.

3. **Unbiased Autoclave**
   A total of 231 AH103 devices (3 lots) passed Unbiased Autoclave with no failures or anomalies. It was necessary to clean the leads of the devices after the Autoclave exposure so that good DC and RF contact could be made.

4. **Unbiased High Temperature Storage**
   A total of 77 AH103 devices (1 lot) passed Unbiased High Temperature Storage with no failures or anomalies.

5. **ESD**
   CDM: A total of 15 AH103 devices were tested at levels of 100, 200, 500, 1000, and 2000 Volts 3 devices per voltage. There was no degradation of performance up to and including the 500V exposure. At 1000 and 2000 Volts, high current and highly degraded RF performance caused device failure. The resulting CDM ESD JEDEC Standard JESD22-C101 classification for the AH103 is a **Class III device** (Highest Voltage Level Passed between 500V and 1000V).

   HBM: A total of 15 AH103 devices were tested at levels of 100, 200, 500, 1000, and 2000 Volts 3 devices per voltage. There was no degradation of performance up to and including the 500V exposure. At 1000 and 2000 Volts, high current and highly degraded RF performance caused device failure. The resulting HBM ESD JEDEC Standard JESD22-A114 classification for the AH103 is a **Class 1B device** (Highest Voltage Level Passed between 500V and 1000V).

6. **Physical Dimensions**
   A total of 10 AH103 devices passed inspection with no failures. All dimensions are within the industry standard tolerances for the SOIC-8 package type.

7. **Solderability**
   A total of 3 AH103 devices passed inspection with no failures.

8. **Highly Accelerated Temperature and Humidity Stress Test (HAST)**
   77 devices from each of three lots for a total of 231 AH103 devices completed 96 hours of HAST. The devices were operated at a "pinchoff" where the gate voltage to each of the die was set at –2.0 V so that Idss was limited. The drain voltage for the HD03 die was set at +5 Volts and the drain voltage for the HD07 die was set at +9 Volts.

   For the three lots, there were no failures; however one device was disqualified from the test. An inductor serving as the bias choke on the PCB went open during the test thereby invalidating the AH103 device it was connected to. Each of the individual AH103's on the PCB has bias inductors serving to provide bias to the device without disturbing the RF performance. The disqualified part was found to be operational within the qualification specification requirements. The cause of the inductor failure was due the HAST exposure and was not related to the operation of the AH103 device it was connected to. One disqualification from a single lot sample of 77 parts, meets the WJCI requirement of LTPD** = 5 for this test. The other two lot samples exhibited no failures.

9. **High Temperature Operation Life (HTOL)**
   A total of 231 AH103 devices (3 lots) passed High Temperature Operation Life with no failures or anomalies.

VII. CONCLUSIONS

The tests performed in this Qualification effort were selected in compliance with industry standards as set forth by the JEDEC. It is accepted in the industry that the successful completion of these tests demonstrates that the semiconductor materials, processes, and techniques used in manufacture of the WJ AH103 have met requirements that establish a level of confidence for the long-term reliability and performance of the device in real life application.

As summarized in this qualification report, the WJ AH103 has successfully met this goal.